LAB 10: BJT Common Emitter

Voltage Divider Biasing

**Date: Reg-No : 2019-EE-360**

**2019-EE-364**

**2019-EE-366**

## OBJECTIVES:

* To determine the quiescent operating conditions of the voltage divider bias BJT configurations.

## SUGGESTED READING:

* Class Lectures
* [Chapter 7: “***Bipolar Junction Transistors***”, *introductory Electronic Devices and Circuits by Robert T. Paynter.*](http://arduino.cc/en/Guide/HomePage)
* Datasheet: 2N3904 NPN bipolar Junction Transistor

Please read through all the suggested reading before you come to lab.

## EQUIPMENT AND COMPONENTS:

* Basic Circuits Training Board
* 2N3904 Transistor
* Jumper Wires
* Palm Scope / DMM
* Resistors
* DC Power Supply

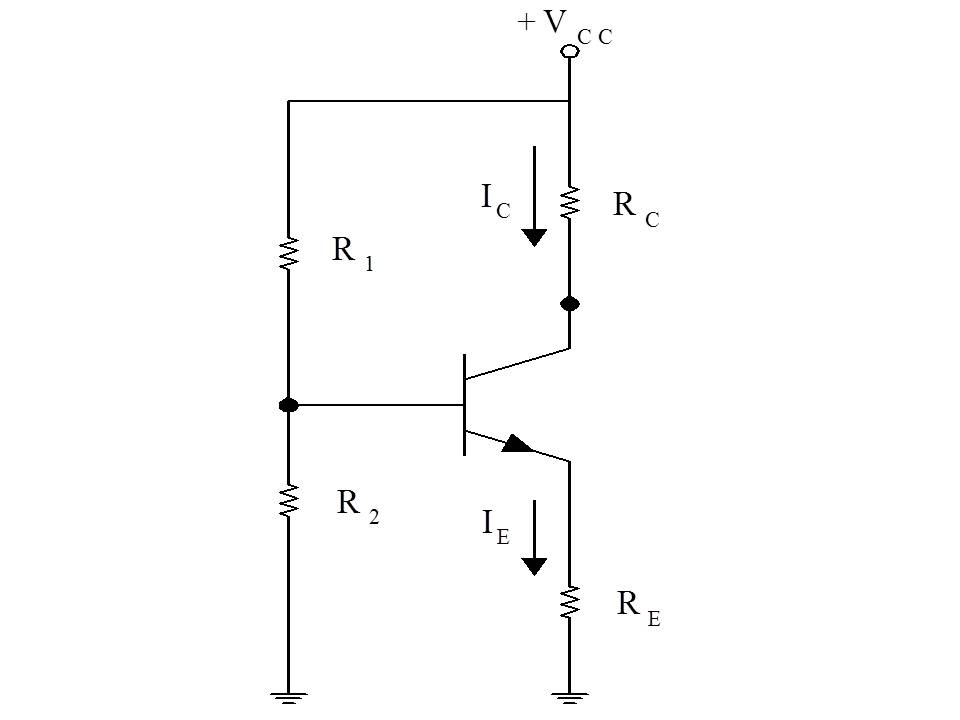
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## Biasing of voltage divider common emitter BJT

Bipolar transistors operate in three modes: cut-off, saturation, and linear. In each of these modes, the physical characteristics of the transistor and the external circuit connected to it uniquely specify the operating point of the transistor. In the cut-off mode, there is only a small amount of reverse current from emitter to collector, making the transistor akin to an open switch. In the saturation mode, there is a maximum current flow from collector to emitter.

The amount of that current is limited primarily by the external network connected to the transistor; its operation is analogous to that of a closed switch. Both of these operating modes are used in digital circuits.

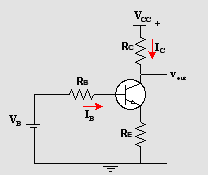
For amplification with a minimum of distortion the linear region of the transistor characteristics is employed. A DC voltage is applied to the transistor, forward-biasing the base emitter junction and reverse-biasing the base-collector junction, typically establishing a quiescent point near or at the center of the linear region.

In this experiment, we will investigate the voltage-divider bias configuration. The fixed biasing has the serious drawback that the location of the q-point is very sensitive to the forward current transfer ratio (β) of the transistor and temperature. Because there can be wide variations in beta and the temperature of the device, it can be difficult to predict the exact location of the Q-point on the load line of a fixed bias configuration.

The voltage divider bias network employs a feedback arrangement that makes the base-emitter and collector emitter voltages primarily dependent on the external circuit elements and not the beta of the transistor. Thus, even though the beta of individual transistors may vary considerably, the location of the Q-point on the load line will remain essentially fixed. The phrase “beta-independent biasing” is often used for such an arrangement.

Fig. *Common emitter voltage divider biasing*

## Input and output current

First of all, the Thevenin resistance or base resistance can be calculated by solving the parallel combination of the resistance and . The voltage at the base of the BJT can be determined by applying the voltage divider rule as given below:

To obtain the expression for the base current we first write the KVL equation

Fig. *Thevenin equivalent of a voltage divider biasing circuit*

Substituting and solving for , we obtain

The above expression has to be multiplied by to obtain the emitter current .

Similarly, the output current (collector current) can be obtained by the following equation

where is the current amplification factor.

## Input and output voltage

The input voltage is base-emitter voltage which is approximately for silicon transistor. The output voltage can be calculated by applying KVL to the output side of the circuit diagram.

where and is the voltage drop across the collector resistance and the emitter resistance respectively.

The voltage drop across both the resistances is given by the following expression

and

Using these equations give the output voltage as

The output voltage can be simply be interpreted as the voltage equal to the supply voltage Vcc minus the voltage that has dropped across the external bias resistors ().

## Procedure

* Connect the circuit as shown in the figure and set the supply voltage Vcc.
* Measure the input current (base current), emitter current and the output current (collector current) with the help of an ammeter. Also calculate all the currents. Record the readings in the table given below.
* Measure the voltage drop across all the external bias resistors and the output voltage VCE with a voltmeter. Also calculate all the voltages. Write them in the table.

## Observations

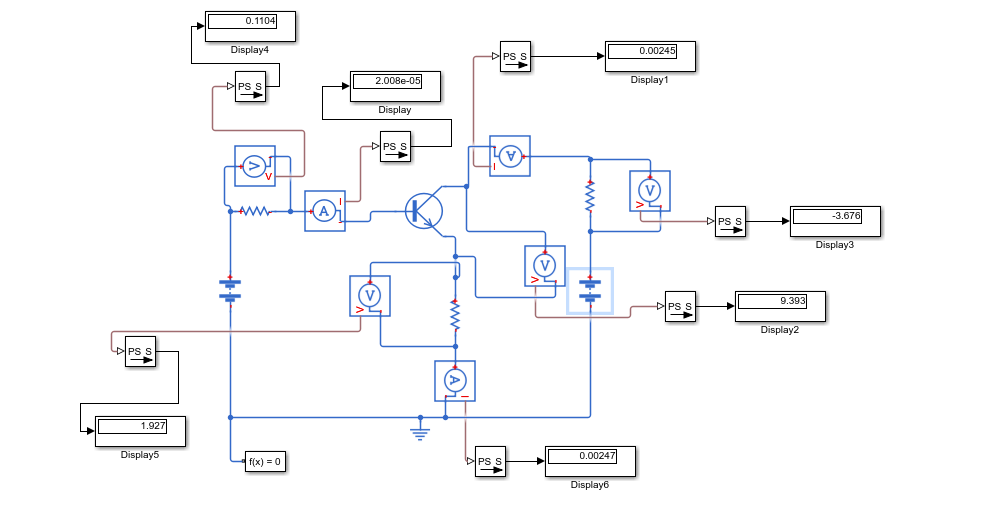
Vcc = \_15 V\_\_, = \_\_33 kΩ\_\_\_, = \_\_6.6 kΩ\_, = 1.5 kΩ\_, = \_780 Ω\_\_

|  |  |  |
| --- | --- | --- |
|  | Calculated | Measured |
| Current Amplification factor | 100 | 100 |
| Base Voltage | 2.5 V | 0.14 V |
| Emitter Voltage | 1.65 V | 1.92 V |
| Collector Voltage | 3.15 V | 3.67 V |
| Output Voltage (VCE) | 10.19 V | 9.393 V |
| Base Current | 0.021 mA | 0.02 mA |
| Collector Current | 2.1 mA | 2 mA |
| Emitter Current | 2.121 mA | 2.4 mA |

## Tasks

* Perform all the calculations for the corresponding currents and voltages on separate pages.

## MATLAB simulation and results



Vcc = \_\_15 V\_\_\_, = \_33 kΩ\_\_\_\_, = \_\_6.6 kΩ\_\_, = \_1.5 kΩ\_\_\_, = \_780 Ω

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# REVIEW QUESTIONS:

Q: How the above configuration that you have implemented in this lab is insensitive or independent of the variations?

In above circuit RB is much greater than RE. So, we can neglect